REMARKS

Claims 1-27 are pending in the present application.

This Amendment is in response to the Office Action mailed March 21, 2000. In the Office Action, the Examiner objected to the abstract, objected to the drawings, provisionally rejected Claims 1-27 under 35 U.S.C. § 101 for double patenting, and rejected Claims 1-27 under 35 U.S.C. § 102. Applicant has amended Claims 1, 11, and 21. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

I. TITLE

In the Office Action, the examiner objected to the title. In particular, the Examiner stated that the title of the invention is neither descriptive nor precise. In response, Applicant has amended the title to change to -- OPTIMIZING CIRCUIT DESIGN PARAMETERS USING A PARAMETER FUNCTION TO SATISFY DESIGN CONSTRAINTS.--

Therefore, Applicant respectfully requests the objection to the title be withdrawn.

II. ABSTRACT

In the Office Action, the Examiner objected to the Abstract. In response, Applicant has amended the Abstract to remove superfluous language. Therefore, Applicant requests the objection to the Abstract be withdrawn.

III. DRAWINGS

In the Office Action, the drawings were objected to by the Draftsperson as noted in the form PTO 948. Applicant shall postpone his submission of formal drawings until the Claims have been allowed.

IV. REJECTIONS UNDER 35 U.S.C. § 101

In the Office Action, the Examiner provisionally rejected Claims 1-27 under 35 U.S.C. § 101 as claiming the same invention as that of claims 1-30 of co-pending Application No. 09/474,008. Applicant respectfully traverses the provisional rejection for the following reason.

A reliable test for double patenting under 35 U.S.C. § 101 is whether a claim in the application could be literally infringed without literally infringing a corresponding claim in the patent. *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970). If there is an embodiment of the invention that falls within the scope of one claim, but not the other, then identical subject matter is not defined by both claims and statutory double patenting would not exist. MPEP 804 II.A. Here, as amended, independent Claims 1, 11, and 21 recite "creating parameter functions" and "optimizing design parameters based on the parameter functions" which are not covered in any of the Claims 1-30 in the co-pending Application No. 09/474,008.

Therefore, Applicant respectfully requests the rejection based on the statutory double patenting be withdrawn.

V. REJECTIONS UNDER 35 U.S.C. § 102

In the Office Action, the Examiner rejected Claims 1-27 under 1) 35 U.S.C. § 102(e) as clearly anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S. Patent No. 5, 880,967 issued to Jyu et al. ("Jyu"), 2) under § 102(a) as being clearly anticipated by U.S. Patent No. 5,835,380 issued to Roething ("Roething") and 3) under § 102(b) as being clearly anticipated by U.S. Patent No.5,619,420 issued to Breid ("Breid"). Applicant respectfully traverses the rejections for the following reasons.

Sarin discloses a technique for modeling, characterization and simulation of integrated circuit power behavior. The technique characterizes both the static and dynamic power consumed by a cell for different logic state conditions on all its ports. (Sarin, Col. 2, lines 15-18). There is no parameter function that represents a relationship among design parameters.

Jyu discloses a minimization of circuit delay and power through transistor sizing. The technique uses a search and select engine. The technique generates a delay and power report for each one of the three circuits, original and two derivations. (Jyu, Col. 6, lines 24-32). There is no parameter function for each of the circuits in a subsystem.

Roething discloses a simulation based extractor of expected waveforms for gate-level power analysis tool. The technique includes a simulation step followed by an iterative process to extract power information (Roething, Col. 4, lines 45-51). The technique, therefore, merely determines power information of a circuit, and does not determine optimal values of design parameters.

Breid discloses a technique to define a semiconductor cell during a layout process of an integrated circuit. The propagation delay is characterized in terms of window factor and cell output loading (Breid, Col. 6, lines 59-64). There are no parameter functions and optimizing design parameters.

Sarin, Jyu, Roething and Breid, taken alone or in any combination, do not disclose, suggest, or render obvious create parameter functions for the plurality of circuits in the subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits. This aspect of the invention is supported in the specification on page 18, lines 6-23, page 19 (lines 1-11), and is recited in the amended Claims 1, 11, 21, and 22.

Therefore, Applicant believes that independent Claims 1, 11, 21 and their respective dependent Claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. § 102(b) and § 103(a) be withdrawn.

CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that the pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: June 21, 2000.

Rose Dunne — 06/21/00
Rose Dunne — *Date*